Sarcouncil Journal of Engineering and Computer Sciences

ISSN(Online): 2945-3585

Volume- 05| Issue- 03| 2026

Research Article **Received:** 01-02-2026| **Accepted:** 25-02-2026 | **Published:** 12-03-2026

Superconducting Qubits: An Evaluation of Architectures, Noise Sources, and Quantum Error Correction Strategies

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Abstract: Superconducting qubits are a leading platform for quantum computation, yet decoherence and scalability challenges continue to limit progress toward fault-tolerant systems. This review synthesizes research on architectures, noise sources, and error correction to clarify performance trade-offs and guide development. The transition from Transmon to Fluxonium has dramatically improved qubit performance, achieving millisecond-scale coherence times. However, this success reveals a fundamental limit of coherence now being primarily restricted by the physical properties of the materials, specifically dielectric losses occurring at the Josephson junction leads and within the surrounding materials. As overcoming these material limits becomes increasingly difficult, system-level engineering determines whether high-coherence qubits can scale.Scaling quantum systems is difficult because current cooling and control systems create too much heat and this forces a shift to integrated digital superconducting circuits and cryogenic light-based links. While these hardware challenges restrict scaling, experiments in error correction show that logical qubits can already outperform physical ones. For example, a distance-7 surface code improved logical qubit lifetime by 2.4×. Achieving practical fault tolerance, however, requires moving beyond simple error models. Future systems must combine techniques like Dynamical Decoupling and Machine Learning-based Optimal Control with dynamic classical control capable of handling complex, correlated faults such as Multi-Bit Burst Errors. Progress in materials, cryogenic system integration for control, and adaptive error management must advance together to realize scalable, high-fidelity quantum hardware.

Keywords: Superconducting qubits, quantum noise sources, quantum error correction, quantum computing, Transmon, Fluxonium.

INTRODUCTION

Superconducting qubits have emerged as one of the leading platforms for quantum computing due to qualities like their fast gate speeds and compatibility with integrated superconducting electronics (Devoret, M., & Martinis, J. 2025; Kjaergaard, M. *et al.,* 2020). A wide variety of superconducting-qubit architectures now exist each promising different trade-offs in coherence and scalability (Siddiqi, I. 2021). Despite these advances, quantum processors struggle with persistent decoherence and instability issues that compromise gate quality and hinder the development of larger qubit architectures (Devoret, M., & Martinis, J. 2025).

Decoherence, the loss of a qubit's quantum properties due to interactions with its environment, arises from multiple physical, often interacting mechanisms (Gambetta, J. M., *et al.*, 2017). Dielectric loss arising from surface defects, oxides, and amorphous materials is one of the most significant contributors to energy relaxation and dephasing in modern quantum devices (Gambetta, J. M., *et al.*, 2017; de Graaf, S. E. *et al.*, 2016). Magnetic flux noise, microscopic two-level fluctuators, charge noise, and coupling-induced crosstalk further introduce instability and time-dependent noise that complicate device calibration and long-term operation (de Graaf, S. E. *et al.*, 2016; Schlör, S. *et al.*, 2016). As qubit arrays grow larger, error management becomes a central challenge for achieving fault-tolerant quantum computation as these noise mechanisms become more complex.

In response to these challenges, several quantum error correction (QEC) strategies and materials-engineering innovations have been innovated. Improvements such as optimized surface encapsulation and substrate treatments have demonstrated significant coherence gains in superconducting qubit transmon devices (Bal, M., *et al.*, 2024). Nevertheless, the published literature on superconducting qubits remains highly fragmented. Studies differ in qubit architecture, fabrication processes, coherence metrics and error-correction approaches. This heterogeneity complicates efforts to compare reported performances across experiments or to draw general conclusions about which design/error-mitigation strategies are reliably effective. As a result, there is no consensus on which superconducting-qubit configurations are truly scalable or ready for large-scale fault-tolerant systems, and little clarity about the relative merits of different QEC or mitigation strategies under realistic noise conditions.

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DOI- https://doi.org/10.5281/zenodo.18988637

Therefore, to provide clarity and support future development, we perform a systematic review that synthesizes work across architectures, noise characterization studies, and error-correction demonstrations. Our goals are to:

- map current design trends and material/fabrication strategies
- catalog dominant noise sources and their measured impact on coherence
- evaluate existing QEC and noise-mitigation experiments in superconducting platforms
- recommend standardized benchmarking practices and research directions to guide scalable, high-fidelity quantum hardware development.

METHODOLOGY

The methodology outlines the research design, data sources and collection strategies, eligibility screening and ethical considerations. This ensures a comprehensive and transparent synthesis of findings.

Research Design

This study employed a systematic review design to consolidate empirical research on superconducting-qubit architectures, noise mechanisms, and quantum error-correction (QEC) strategies. This approach enabled the identification of recurring themes and understudied areas to guide future research and practical applications.

Data Sources and Collection Strategies

A structured literature search was conducted across four major research databases: *ResearchGate, arXiv, IEEE Xplore and MDPI* which are widely used for disseminating quantum-engineering and superconducting-device research. Search terms were selected to capture the three aforementioned domains of architectures, noise sources, and error correction. This included combinations such as, but not limited to, "superconducting qubits," "quantum error correction," and "materials engineering for qubits".

Eligibility Criteria

The review includes 31 studies (peer-reviewed journal articles, conference papers, preprints, and technical reports) published between 2010 and 2025.

Inclusion Criteria

- Peer-reviewed journal articles, conference proceedings, preprints with empirical data, technical reports, or book chapters published between 2010 and 2025.
- Studies reporting experimental results on superconducting qubits (e.g., coherence times, gate fidelities, noise measurements) or experimental demonstrations of quantum error correction (QEC) or error-mitigation on superconducting platforms.
- Theoretical and simulation studies that directly analyze device-level noise, materials interfaces, or QEC performance under realistic noise models and that provide extractable, comparable metrics.

Exclusion Criteria

- Non-English language publications.
- Papers published before 2010.
- Purely theoretical works that do not present device-relevant simulations or extractable metrics (i.e., conceptual-only papers without numerical/experimental evidence).
- Opinion pieces, editorials, or blog posts lacking empirical or simulation data.

Ethical Considerations

This review used only publicly available scientific literature and did not involve human subjects or proprietary datasets. Ethical review was therefore not required, following precedents in systematic reviews of quantum-computing and superconducting-device research.

RESULTS AND FINDINGS

Comparative Evaluation of Superconducting Qubit Architectures

The development of superconducting quantum computers is critically dependent on the selection of optimal qubit architectures that balance intrinsic coherence with control complexity and scalability. Current research highlights the fundamental trade-offs between the established Transmon design and the high-coherence Fluxonium variant, leading toward highly specialized hybrid systems. A schematic comparison of the Transmon and Fluxonium qubit types is as shown below with Figure 1:

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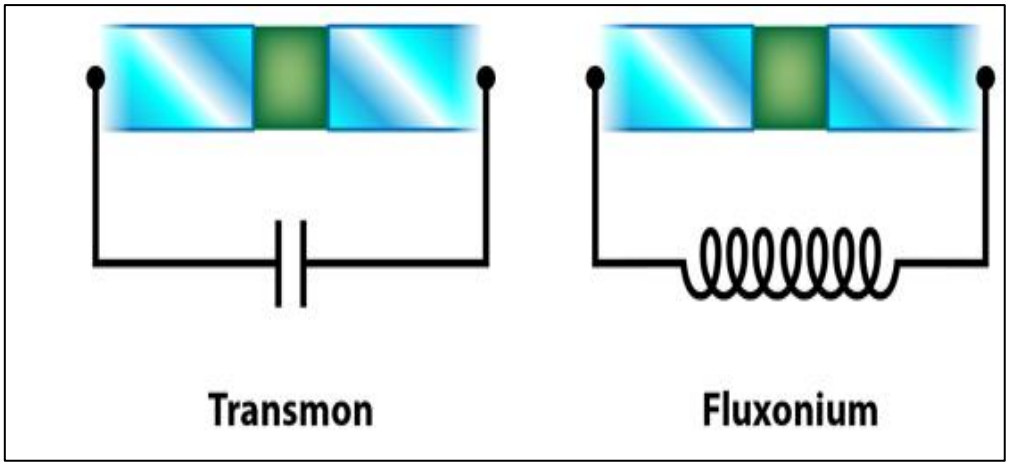

Figure 1 : Schematic Comparison of Transmon and Fluxonium Qubit. Adapted from G. Catelani, "Fluxonium Steps up to the Plate", Physics 12, 131 (2019), APS.

Performance Metrics and Limitations of Transmon Qubit Architecture

The Transmon qubit, derived from a capacitively-shunted charge qubit, remains a cornerstone architecture due to its straightforward design, ease of fabrication, and compatibility with initial scalable integration efforts (Somoroff, A. *et al.*, 2023). It was the foundational element for early demonstrations of quantum supremacy and lattice-based error correction implementations [9]. Despite these advantages, the Transmon faces significant architectural limitations that cap its performance ceiling. Typical uncorrected T_2 coherence times are restricted to the range of tens to hundreds of microseconds (Somoroff, A. *et al.*, 2023). A major factor limiting the Transmon's fidelity is its susceptibility to environmental disturbances, particularly dielectric noise, and its inherently weak anharmonicity. This small anharmonicity dictates that gate operations cannot be arbitrarily fast; spectrally broad control pulses risk exciting transitions to non-computational (leakage) states (Somoroff, A. *et al.*, 2023; Solgun, F. *et al.*, 2019). Furthermore, the Transmon design is highly sensitive to coupling with Two-Level Defects (TLS), which are responsible for frequency shifts and limiting both the relaxation time (T_1) and dephasing time (T_2) (Schlör, S. *et al.*, 2019). Consequently, while simple, the Transmon architecture struggles to maintain the ultra-low error rates necessary for practical fault-tolerant operation. Here, T_1refers to the time scale over which an excited qubit decays to its ground state. T_2 refers to the time scale over which a qubit loses phase coherence, i.e. the stable relationship between its quantum states becomes disturbed by noise.

Performance Metrics and Limitations of Fluxonium Qubit Architecture

The Fluxonium qubit, characterized by a large shunt inductance, was introduced to circumvent the limitations imposed by circuit-specific noise sources in the Transmon. By introducing a large inductance, the Fluxonium significantly enhances resilience against dielectric noise, providing a less exploited yet increasingly popular qubit type (Place, A. P. M. *et al.*, 2021). This architectural improvement has resulted in exceptional T_2 coherence metrics. Fluxonium qubits have been reported to achieve uncorrected coherence times of up to 1.48 ± 0.13 milliseconds. This represents an order-of-magnitude leap beyond the typical coherence times observed in Transmon devices (Somoroff, A. *et al.*, 2023). Furthermore, the improved noise resilience facilitates extremely high gate quality, with average single-qubit gate fidelity benchmarked at 0.99991. This evidence demonstrates that the Fluxonium design successfully suppresses circuit-level noise contributions. However, even at these millisecond coherence levels, the ultimate performance is noted to be limited by fundamental material absorption (Nguyen, L. B. *et al.*, 2019). This observation implies that the research focus is shifting from optimizing quantum circuit topology to addressing the intrinsic physics of the solid-state materials themselves.

Scalability, Crosstalk, and Hybrid Architectures

Scaling up quantum processors requires minimizing residual coupling (the persistent unwanted interaction between neighboring qubits) also known as crosstalk. Of particular concern is the ZZ interaction, a specific type of coupling where the computational states of adjacent qubits

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influence each other's energy levels (Lange, F. *et al.*, 2025). Transmon lattices often experience challenges related to high crosstalk. Fluxonium architectures, however, show strong suppression of residual ZZ interactions, even in larger lattices that incorporate tunable Transmon couplers (Lange, F. *et al.*, 2025; Lange, F. *et al.*, 2025). This resilience suggests that Fluxonium lattices, when designed to achieve similar gate speeds and fidelities as Transmons, may offer inherently lower crosstalk. To maximize performance while mitigating the complex control requirements often associated with high-coherence designs, dual-species architectures are being actively explored (Dimitrov, N. D. *et al.*, 2025). In these systems, Fluxonium qubits serve as the highly coherent computational qubits, while fixed-frequency Transmon qubits are used as ancillas to facilitate fast, high-fidelity operations like controlled-Z gates and high-speed readout. This strategy consolidates critical functions into a single ancilla, establishing the viability of a dual-species system as a promising pathway toward scalable, fault-tolerant quantum computation (Dimitrov, N. D. *et al.*, 2025). This evolution confirms that architecture selection is increasingly about integrating specialized components into a heterogeneous system optimized for both noise resilience and control efficiency.

Table 1: Comparison of Qubit Architectures

Parameter	Transmon	Fluxonium	Key Trade-Off / Advantage
Max Uncorrected T_2^* (Range)	Tens to hundreds of μ seconds	Up to 1.48 milliseconds	Coherence: Fluxonium offers an order-of-magnitude increase
Anharmonicity ($\alpha/2\pi$)	Small ($\sim 250MHz$)	Large	Control: Floxonium offers better suppression of leakage states during fast gates.
Primary Scaling Challenge	High Crosstalk, Dielectric Defects	Increased Fabrication Complexity	Scalability: Hybrid designs mitigate complexity while Fluxonium suppresses crosstalk
Ultimate Performance Limit	Surface loss / Dielectric defects	Material absorption	Mitigation strategies are converging on materials science solutions

Physical Mechanisms and Impact of Noise Sources

Understanding the quantitative contribution of various noise sources is essential for driving targeted material and design improvements. Qubit decoherence is overwhelmingly dominated by losses originating from defects within the solid-state environment.

The Role Of Dielectric Loss and Two-Level Systems (TLS)

Energy relaxation (T_1) in superconducting qubits is fundamentally limited by dielectric losses associated with the tunneling Two-Level Systems (TLS) present in amorphous layers and interfaces (Gambetta, J. M. *et al.*, 2017). A key finding challenges the traditional focus on large capacitive areas as the primary source of loss. Finite-element simulation and subsequent experimental validation have determined that the dominant surface loss contribution in Transmon qubits often originates from the Josephson junction wiring leads (Smirnov, N. S. *et al.*, 2024). This highly localized loss contribution can account for over 50% of the total surface loss. This realization compels circuit designers to shift their focus to rigorous optimization of these micro-features, leading to practical gains such as up to 20 % improvement in the qubit quality factor achieved through wiring design optimization (Smirnov, N. S. *et al.*, 2024).

Low-Frequency Noise and Its Impact on Qubit Coherence

The primary determinant of the uncorrected dephasing time (T_2) is the nature of low-frequency noise. Measurements of the spectral density of qubit frequency fluctuations consistently show dominance by pink noise (1/f) (Tan, Y. P. *et al.*, 2025). This noise is attributed to microscopic fluctuations associated with charge, flux, and TLS defects in the solid-state device (Tan, Y. P. *et al.*, 2025). By comparison, white noise, which may stem from thermal noise or control setup electronics, is a secondary contributor, with control system frequency drift measured to be insignificant (approximately ± 0.2Hz). When dephasing noise is suppressed using advanced techniques like spin-echo or CPMG sequences, the resulting T_2 is often observed to be limited by T_1, meaning $T_2 \cong 2\,T_1$ (Burnett, J. J. *et al.*, 2019). This indicates that in well-engineered systems, the ultimate coherence floor is set by the energy

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relaxation time, emphasizing the continued importance of material science in improving T_1.

Now that the major noise sources have been identified, it becomes clear that achieving high-fidelity qubit performance requires more than a single type of intervention. Proactive methods are needed to suppress errors at their origin by shaping qubit dynamics and reducing their exposure to environmental fluctuations. At the same time, reactive methods must be used to detect and correct the errors that inevitably remain to ensure that quantum information can be preserved over long periods. Together, these complementary strategies form the foundation for reliable quantum operation.

Engineering Strategies For Error Suppression and Control

Fault-tolerant computation begins at the physical layer: errors must be suppressed before they can be corrected. This section focuses on these proactive, hardware-level strategies that reduce noise at its origin through improved pulse engineering and cryogenic control stability.

Advanced Pulse Sequences for Error Mitigation

Non-QEC techniques enhance the intrinsic quality of quantum gates, reducing the resource overhead required by subsequent error correction.

Dynamical Decoupling (DD): *DD* sequences apply precise pulse trains to actively decouple the qubit from environmental noise, effectively extending coherence times (Sud, J. *et al.*, 2022). *DD* is particularly useful for suppressing the dominant 1/f noise component underlying single-qubit decoherence (Evert, B. *et al.*, 2025). Beyond mitigating incoherent noise, tailored *DD* sequences are used to characterize and suppress coherent errors, notably static *ZZ* coupling between qubit pairs. Specific sequences, such as syncopated *DD*, have been demonstrated to selectively target unwanted two-qubit interactions, leading to a significant boost in performance within realistic algorithmic circuits (Evert, B. *et al.*, 2025). Furthermore, *DD* can be inserted into cycles containing two-qubit gates to mitigate crosstalk arising from neighboring operation.

Quantum Optimal Control (QOC): *QOC* methods (e.g., GRAPE and Krotov) optimize the shape and timing of microwave pulses to achieve operations with the highest possible fidelity and shortest duration (Genois, É. *Et al.*, 2025). These methods typically rely on accurate physical modeling of the device (Matekole, E. S. *et al.*, 2022). A significant advancement is the use of Machine Learning-based QOC (*MLQOC*), where physics-inspired machine learning infers an accurate model of the device dynamics directly from experimental data (Genois, É. *Et al.*, 2025). This approach allows for the optimization of control pulses against real-world model bias (i.e., out-of-model dynamics not captured by the theoretical Hamiltonian), achieving high single-qubit gate fidelities of approximately 0.9999% in simulation under realistic conditions (Genois, É. *Et al.*, 2025). The ability of *MLQOC* to adaptively compensate for systematic hardware imperfections makes it an indispensable tool for achieving the threshold fidelities required for fault tolerance.

The Cryogenic Stability Bottleneck

The scaling of superconducting quantum processors to millions of qubits is predominantly hindered by the interface between room-temperature control electronics and the millikelvin cryogenic environment. The limited cooling power of dilution refrigerators severely restricts the acceptable heat load from control wiring and cabling (Joshi, S., & Moazeni, S. 2024). To overcome this scaling challenge, two key technological shifts are underway:

Cryogenic RF-Photonic Systems: One promising solution focuses on scaling the necessary XY-control lines using cryogenic RF-photonic links. This method leverages advanced silicon photonic processes and Wavelength Division Multiplexing (WDM) to multiplex control signals, drastically reducing the physical cable count and managing the heat load from passive and active components (Joshi, S., & Moazeni, S. 2024). This solution is modeled to achieve a scale-up toward a thousand-qubit control interface.

Integrated Digital Superconducting Logic: An alternative is to integrate high-speed, low-power digital Single Flux Quantum (SFQ) circuits directly at base temperature (Joshi, S., & Moazeni, S. 2024). These SFQ circuits implement the quantum-classical interface, generating coherent pulse sequences for qubit control and enabling projective measurement using Josephson photon counters. By moving signal processing into the cryogenic stage, this approach bypasses the complex rack-full of room-temperature microwave infrastructure, allowing for a far more compact and scalable quantum computing infrastructure (Joshi, S., & Moazeni, S. 2024). The reliance on these specialized photonic and digital superconducting technologies confirms that scaling is a

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heterogeneous integration challenge demanding expertise beyond conventional microwave control.

Experimental Progress in Quantum Error Correction (QEC)

While physical-layer techniques reduce the rate at which errors occur, they cannot eliminate noise entirely. To achieve truly reliable computation, these remaining faults must be detected and corrected at the logical level. This section turns to that logical layer and explains how QEC provides the mechanisms needed to bridge the gap between noisy physical qubits and fault-tolerant, large-scale computation. Figure 2 illustrates the standard QEC workflow, where ancilla qubits interact with data qubits to generate a syndrome, the syndrome is measured, and a classical decoder determines the appropriate correction to restore the encoded quantum state. Recent experiments have confirmed the viability of both active and passive QEC strategies in superconducting circuits, reaching the critical break-even point (the moment when an encoded logical qubit's lifetime or error rate becomes better than the best individual physical qubit used to create it).

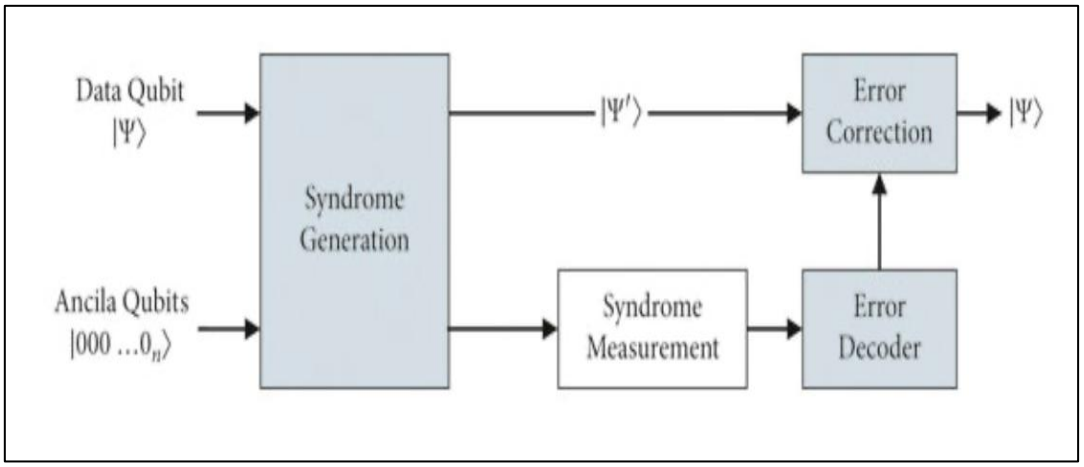

Figure 2: General Quantum Error-Correction (QEC) workflow showing syndrome generation, measurement, decoding and correction. Adapted from Khalifa et al "Digital System Design for Quantum Error Correction Codes", ResearchGate (2021)

Achieving Break-even with Active and Passive QEC

The fundamental requirement for QEC is that the logical qubit memory lifetime must exceed the lifetime of its best physical constituent qubit. This milestone has been successfully demonstrated in superconducting hardware.

Active QEC (Surface Codes): Large-scale experiments using the topological surface code have achieved significant results. A demonstration using 17 physical qubits in a superconducting circuit achieved fast ($1.1\,\mu s$) and high-performance QEC cycles (Shirol, S. *et al.,* 2025). More critically, a distance-7 surface code implemented using 101 physical qubits successfully demonstrated a logical memory lifetime that exceeded the lifetime of the best physical qubit by a factor of 2.4 ± 0.3. The logical error rate per cycle for this demonstration was reported as $0.143 \pm 0.003\%$.

Passive QEC (Continuous Stabilization): Research has also validated the quantitative competitiveness of continuous, passive correction strategies that circumvent some demanding hardware requirements of active stabilization (Othman, A. 2019). A steady-state driven dissipative quantum system, which employs a superconducting cavity and a Transmon ancilla using a binomial encoding, was demonstrated to preserve a logical qubit state beyond the photon-lifetime limit by approximately 5% (Shirol, S. *et al.,* 2025). This demonstrates that autonomous stabilization is a viable method for error resilience.

Mitigating External and Correlated Faults

As quantum processors increase in size, their vulnerability to non-local, correlated fault sources increases. Natural radiation is a source of high-sensitivity faults that can induce Multi-Bit Burst Errors (MBBEs), potentially undermining standard QEC protocols designed primarily for local, stochastic errors (Vallero, M. *et al.,* 2024).

To maintain resilience against these external threats, systems must incorporate dynamic error mitigation. One proposed architecture, Q3DE, enhances fault tolerance by integrating in-situ anomaly detection (Suzuki, Y. *et al.,* 2022). Upon

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detection of an MBBE from syndrome data, Q3DE initiates dynamic code deformation, which temporarily increases the encoding level of the logical qubit. Simulations indicate that this method effectively reduces the period of MBBEs by 1000 times. Further analysis suggests that optimizing the surface code parameters based on the anticipated physical fault model can increase the probability of correcting radiation-induced faults by up to 10% without adding physical overhead (Vallero, M. *et al.*, 2024). These findings confirm that future Fault-tolerant Quantum Computing (FTQC) systems must incorporate classical resilience engineering techniques to manage external and correlated noise effectively.

DISCUSSION AND RECOMMENDATIONS

The pursuit of scalable, fault-tolerant quantum computing faces interconnected challenges spanning materials and logical qubit performance. In this section, we provide a focused overview of these challenges before presenting targeted recommendations to guide future research and development in these areas.

The Materials Barrier to Coherence

The progression from Transmon to Fluxonium architectures has pushed superconducting qubit performance to the millisecond coherence regime. However, this improvement has merely exposed a deeper, universal constraint: the coherence limit is now determined by the fundamental material properties, such as dielectric losses and material absorption. This situation dictates that further breakthroughs will rely less on quantum circuit theory and more on materials science innovations. The success of techniques like niobium surface encapsulation and acoustic bandgap engineering (Bal, M. *et al.*, 2023; Chen, M. *et al.*, 2024) confirms that the next generation of performance gains must be achieved by systematically eliminating the physical defects that govern the limit. Furthermore, the identification of microscopic features, specifically Josephson junction leads, as dominant loss source (Smirnov, N. S. *et al.*, 2024), proves that ultra-low-loss manufacturing must extend to the nanoscale components of the circuit.

The System Integration Imperative

The fabrication challenge has largely been replaced by the system control challenge. Scaling a quantum computer is now fundamentally a thermal engineering and interface integration problem (Joshi, S., & Moazeni, S. 2024). The volume of control infrastructure required to manage thousands of qubits vastly exceeds the cooling capacity of current cryogenic platforms. The necessary technological solution involves replacing traditional microwave controls with integrated, low-power alternatives: digital superconducting SFQ circuits for base-temperature logic and cryogenic RF-photonic links for high-density, low-heat input/output (I/O). The feasibility of scalable quantum computing is therefore contingent upon achieving resilient, industrial-scale integration of these specialized classical hardware components within the cryogenic environment.

Ensuring Practical Fault-Tolerance Beyond QEC Break-Even

The successful demonstration of QEC break-even, where logical memory lifetimes surpass physical qubit limits (Shirol, S. *et al.*, 2025), validates the fundamental feasibility of fault-tolerant superconducting computation. However, the subsequent focus must shift from simply demonstrating feasibility to ensuring practical resilience. The emergence of research on mitigating correlated faults like MBBEs highlights that the classical control layer must be dynamic and intelligent, capable of adapting the QEC protocol based on real-time noise characterization, thus moving beyond reliance on simplistic, independent-error fault models.

Together, these findings make clear that the path to scalable superconducting quantum computing is no longer defined by a single bottleneck but by the coordinated advancement of materials and system integration. Achieving fault-tolerance at scale will require simultaneous progress across all three fronts of pushing coherence through materials innovation, enabling size through cryogenic integration, and securing reliability through adaptive error management.

Recommendations

On Fabrication and Material

Mandatory Ambient-Stable Passivation: Niobium surface protection (such as adding a thin Tantalum or Gold cap) should be a standard part of fabrication. This would ensure a systematic and reproducible baseline average T_1 lifetime of at least 200 μs across different fabrication facilities.

Nanoscale Loss Mitigation via Advanced Deposition: Research should be directed towards understanding and improving the tiny dielectric and metal interfaces in the most confined parts of

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the device, particularly the wiring around the Josephson junction. Highly controlled deposition methods are needed to reduce the localized losses in these regions, which can contribute over 50% of the total surface loss.

Invest in Phononic Environment Engineering: Research into phononic engineering of the bulk material and substrate, including the use of acoustic bandgap structures, should be increased to physically isolate TLS defects from the qubit. The goal of these phononic approaches would be to suppress unwanted vibrations and energy leakage, enabling T_1 coherence times above 5 milliseconds.

On System Integration

Deep-Cryogenic Digital and Photonic Control: Future investment should focus on integrated cryogenic control systems rather than relying on large amounts of external microwave cabling. This includes using cryogenic RF-photonic links with Wavelength Division Multiplexing (WDM) to deliver dense, low-heat XY control for hundreds or thousands of qubits. At the same time, development should advance high-speed, low-power digital SFQ circuits for quantum-classical interfacing and fast measurement decoding at the coldest stages of the system.

Dynamic QEC Control Layer: Advanced classical control systems that can quickly analyze error syndromes and detect unusual behavior should be developed. These systems should support dynamic coding methods, such as dynamic code deformation Q3DE, to provide real time protection against correlated noise events like MBBEs and to strengthen the reliability of logical qubits.

On Improving Qubit Logical Performance:

Universal Adaptive Error Suppression: High-fidelity, dual-species architectures, with Fluxonium as the computational qubit and Transmon as the ancilla should be increasingly used. Tailored Dynamical Decoupling (DD) sequences should be applied to all circuit operations, including idling and pulsing, to actively reduce single-qubit 1/f and residual static ZZ crosstalk.

Adopt ML-Guided Optimal Control: Machine Learning-based Quantum Optimal Control (MLQOC) should be used as a standard method for gate optimization. This allows the control system to continuously learn the qubit dynamics, correct for systematic model errors, and achieve consistent gate fidelities of 0.9999% or higher, which is needed for resilient QEC performance.

Standardize Logical Performance Reporting: Experimentally measured logical error rates per QEC cycle should be adopted as the main performance metric. These measurements should be validated with advanced methods such as Randomized Benchmarking to provide a clear and computationally meaningful measure of progress toward the fault-tolerance threshold

CONCLUSION

The pursuit of scalable, fault-tolerant superconducting quantum computing faces a tightly coupled trilemma involving materials science, error correction, and adaptive quantum control. Architectural advancements, from Transmon to Fluxonium, have reached a materials-limited performance ceiling. Future gains will require improvements in nanoscale fabrication purity and phononic environment engineering. At the same time, system-level integration must be addressed. Dense, low-power solutions such as SFQ logic and cryogenic RF-photonics are needed to scale processors beyond current thermal limits. Finally, the feasibility of Quantum Error Correction (QEC) must be translated into practical resilience. Intelligent, adaptive control systems can suppress correlated noise and compensate for real-time hardware imperfections using techniques like ML-guided optimal control. Progress in coherence, integration, and reliability must move forward together to achieve truly fault-tolerant quantum computation

REFERENCES

1. Devoret, M., & Martinis, J. "Implementing Qubits with Superconducting Integrated Circuits: Experimental Aspects of Quantum Computing." *Quantum Information Processing* 3 (2005).
2. Kjaergaard, M., Schwartz, M., Braumüller, J., Krantz, P., Wang, J., Gustavsson, S., & Oliver, W. "Superconducting Qubits: Current State of Play." *Annual Review of Condensed Matter Physics* 11 (2020).
3. Siddiqi, I. "Engineering high-coherence superconducting qubits." *Nature Reviews Materials* 6 (2021): 875–891.
4. Gambetta, J. M., et al. "Investigating Surface Loss Effects in Superconducting Transmon Qubits." *IEEE Transactions on Applied Superconductivity* 27.1 (2017): 1–5.
5. de Graaf, S. E., Adamyan, A. A., Lindström, T., Erts, D., Kubatkin, S. E., Tzalenchuk, A.

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Y., & Danilov, A. V. "Direct identification of dilute surface spins on Al_2O_3: Origin of flux noise in quantum circuits." *arXiv preprint* (2016).
6. Schlör, S., Lisenfeld, J., Müller, C., Bilmes, A., Schneider, A., Pappas, D. P., Ustinov, A. V., & Weides, M. "Correlating Decoherence in Transmon Qubits: Low Frequency Noise by Single Fluctuators." *Physical Review Letters* 123.19 (2019): 190502.
7. Bal, M., et al. "Systematic improvements in transmon qubit coherence enabled by niobium surface encapsulation." *npj Quantum Information* 10.1 (2024).
8. Somoroff, A., Ficheux, Q., Mencia, R., Xiong, H., Kuzmin, R., & Manucharyan, V. "Millisecond Coherence in a Superconducting Qubit." *Physical Review Letters* 130 (2023): 267001.
9. Heunisch, L., Huang, L., Tasler, S., Schirk, J., Wallner, F., Feulner, V., Sarma, B., Liegener, K., Schneider, C., Filipp, S., & Hartmann, M. "Scalable Fluxonium-Transmon Architecture for Error Corrected Quantum Processors." *arXiv preprint* (2025).
10. Solgun, F., DiVincenzo, D. P., & Gambetta, J. M. "Simple Impedance Response Formulas for the Dispersive Interaction Rates in the Effective Hamiltonians of Low Anharmonicity Superconducting Qubits." *IEEE Transactions on Microwave Theory and Techniques* 67.3 (2019): 928–948.
11. Schlör, S., Lisenfeld, J., Müller, C., Bilmes, A., Schneider, A., Pappas, D. P., Ustinov, A. V., & Weides, M. "Correlating decoherence in transmon qubits: low frequency noise by single fluctuators." *Physical Review Letters* 123.19 (2019): 190502.
12. Place, A. P. M., Rodgers, L. V. H., Mundada, P., et al. "New material platform for superconducting transmon qubits with coherence times exceeding 0.3 milliseconds." *Nature Communications* 12 (2021).
13. Nguyen, L. B., Lin, Y. H., Somoroff, A., Mencia, R., Grabon, N., & Manucharyan, V. E. "High-Coherence Fluxonium Qubit." *Physical Review X* 9.4 (2019): 041041.
14. Lange, F., Heunisch, L., Fehske, H., DiVincenzo, D., & Hartmann, M. "Cross-talk in superconducting qubit lattices with tunable couplers: Comparing transmon and fluxonium architectures." *arXiv preprint* (2025).
15. Lange, F., O'Keeffe, M., Zhang, L., & Kraglund Andersen, C. "Cross-talk in superconducting qubit lattices with tunable couplers: Comparing transmon and fluxonium architectures." *arXiv preprint* (2025).
16. Dimitrov, N. D., Wang, C., Manucharyan, V. E., & Vavilov, M. G. "Cross-Resonant Gates in Hybrid Fluxonium-Transmon System." *arXiv preprint* (2025).
17. Gambetta, J. M., Murray, C. E., Fung, Y. K. K., McClure, D. T., Dial, O., Shanks, W., Sleight, J., & Steffen, M. "Investigating surface loss effects in superconducting transmon qubits." *IEEE Transactions on Applied Superconductivity* 27 (2017): 1700205.
18. Smirnov, N. S., Krivko, E. A., Solovyova, A. A., Ivanov, A. I., & Rodionov, I. A. "Wiring surface loss of a superconducting transmon qubit." *Scientific Reports* 14.1 (2024): 7326.
19. Tan, Y. P., Yap, Y. S., Nguyen, L. H., Budoyo, R. P., Bore, P., Park, K. H., Hufnagel, C., & Dumke, R. "Characterizing Noise in Controlling Superconducting Qubits." *arXiv preprint* (2025).
20. Burnett, J. J., Bengtsson, A., Scigliuzzo, M., Niepce, D., Kudra, M., Delsing, P., & Bylander, J. "Decoherence benchmarking of superconducting qubits." *npj Quantum Information* 5.1 (2019): 54.
21. Sud, J., Grabbe, S. R., Evert, B., Reagor, M., Hu, H. Y., Gonzalez Izquierdo, Z., Rieffel, E. G., & Wang, Z. "Dynamical Decoupling of Crosstalk on Superconducting Qubit Devices." *NASA Technical Reports Server* (2022).
22. Evert, B., Izquierdo, Z., Sud, J., Hu, H. Y., Grabbe, S., Rieffel, E., Reagor, M., & Wang, Z. "Syncopated dynamical decoupling to suppress crosstalk in quantum circuits." *Physical Review Applied* 24 (2025).
23. Genois, É., Stevenson, N. J., Goss, N., Siddiqi, I., & Blais, A. "Quantum optimal control of superconducting qubits based on machine-learning characterization." *Physical Review Applied* 24 (2025): 034073.
24. Matekole, E. S., Fang, Y. L. L., & Lin, M. "Methods and Results for Quantum Optimal Pulse Control on Superconducting Qubit Systems." *Proceedings of the IEEE International Parallel and Distributed Processing Symposium Workshops* (2022).
25. Joshi, S., & Moazeni, S. "Scaling up Superconducting Quantum Computers With Cryogenic RF-Photonics." *Journal of Lightwave Technology* 42.1 (2024): 166–175.
26. Shirol, S., Geldern, S., Xi, H., & Wang, C. "Passive quantum error correction of photon loss at breakeven." *arXiv preprint* (2025).

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27. Othman, A. "Cat Qubits: A Pathway to Error-Resilient Quantum Information Processing." *ResearchGate preprint* (2019).
28. Vallero, M., Casagranda, G., Vella, F., & Rech, P. "On the Efficacy of Surface Codes in Compensating for Radiation Events in Superconducting Devices." *Proceedings of SC24: International Conference for High Performance Computing, Networking, Storage and Analysis* (2024).
29. Suzuki, Y., Sugiyama, T., Arai, T., Liao, W., Inoue, K., & Tanimoto, T. "Q3DE: A fault-tolerant quantum computer architecture for multi-bit burst errors by cosmic rays." *Proceedings of the IEEE/ACM International Symposium on Microarchitecture* (2022).
30. Bal, M., Murthy, A., Crisa, F., Zhu, S., Lecocq, F., Aumentado, J., Ullom, J., & Hopkins, P. "Systematic Improvements in Transmon Qubit Coherence Enabled by Niobium Surface Encapsulation." *PRX Quantum* (2023).
31. Chen, M., Owens, J. C., Putterman, H., Schäfer, M., & Painter, O. "Phonon engineering of atomic-scale defects in superconducting quantum circuits." *Science Advances* (2024).

Source of support: Nil; **Conflict of interest:** Nil.

Cite this article as:
Njie, M. " Superconducting Qubits: An Evaluation of Architectures, Noise Sources, and Quantum Error Correction Strategies." *Sarcouncil Journal of Engineering and Computer Sciences* 5.3 (2026): pp 22-31.

Publisher: SARC Publisher